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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,087	01/22/2004	Alexander G. MacInnis	17403US05	6408

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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,087	MACINNIS ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/13/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after appeal to the Board of Patent Appeals and Interferences, but prior to a decision on the appeal. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 10/29/2007 has been entered.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 4 – 11 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable claims 1 – 32 of U. S. Patent No. 6,721,837, claims 1 – 22 of U. S. Patent No. 6,189,064, claims 1 – 31 of U. S. Patent No. 7,209,992.

Current Application	US Patent No. 6,189,064	US Patent No. 6,721,837	US Patent No. 7,209,992
Claim 4	1, 3	27	1
Claim 6	8	6	1
Claim 7	1, 3		
Claim 8	2		
Claim 10	9	9	
Claim 11	21, 22		

Although the conflicting claims are not identical, they are not patentably distinct from each other despite different wordings of the time scheduling features, they teach precluding a device or high priority device from accessing the memory, which represents the preventative measures in the current application.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 4 – 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Hook et al. (US Patent Number 6,342,892 hereinafter "Hook").

6. As per claim 4, Hook teaches a unified memory system comprising: a memory (main memory 300, figure 2) that is shared by a plurality of devices including at least a central processing unit (main processor 100, figure 2) and a graphics processing unit (coprocessor 200, figure 2); and a memory request arbiter (memory controller/interface registers, figure 37, column 61, lines 32 – 53) coupled to the memory (allows for memory allocation between the two processors, column 61, lines 32 – 53 and column 14, lines 50 – 63), wherein the memory request arbiter performs real time scheduling of memory requests from different devices having different priorities, the unified memory system provides for real time scheduling of tasks (real time scheduling of tasks in task list, figure 8, column 21, lines 9 – 36), and provides access to memory by requesters that are sensitive to latency and do not have determinable periodic behavior (the requesters do not have periodic behavior as the tasks are generated on an as-needed basis, column 11, lines 36 - 42).

The Examiner notes that the unified memory of Hook "provides" for real time scheduling and access to memory and no teachings in Hook stipulate that the "provide" or provision of the steps of the claim limitations cannot be accomplished by the prior art. There is nothing in the unified memory of Hook to inhibit its ability to provide for real time scheduling and access.

7. As per claim 5, Hook teaches a unified memory system wherein the central processing unit and the graphics processing unit are sensitive to latency and do not have determinable periodic behavior (processing does not have periodic behavior, includes latency register 1060, figure 37E).

8. As per claim 6, Hook teaches a unified memory system wherein a predetermined minimum interval between subsequent accesses by a device is enforced (subsequent access are delayed by predetermined pipelined delay between processes, column 37, lines 7 - 30).

9. As per claim 7, Hook teaches a unified memory system further comprising a circuit component associated with one or more devices and coupled between the associated devices and the memory request arbiter, wherein the circuit component is used to enforce at least a predetermined minimum interval between subsequent accesses by the associated device (task list via memory controller, column 61, lines 14 - 31).

10. As per claim 8, Hook teaches a unified memory system wherein the devices associated with the circuit component include a CPU (CPU 202, figure 6A).

11. As per claim 9, Hook teaches a unified memory system wherein the devices associated with the circuit component make high priority service requests through the circuit component (DMA requests from 210, figure 6a).

12. As per claim 10, Hook teaches a unified memory system further comprising a round robin server for handling low priority tasks (DMA requests from 208, figure 6a).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hook in view of Ottinger (US Patent Number 6,070,231).

15. As per claim 11, Hook teaches a unified memory system comprising a memory controller (memory controller 212, figures 6 and 37), the memory request arbiter

coupled to the memory controller wherein the arbiter perform real time scheduling of memory requests (coupled via interface register 212, figures 6 and 37).

Hook does explicitly disclose a **dual** memory controller.

Ottinger teaches a memory system comprising dual memory controllers (figure 1), the dual memory controllers including a first memory controller (24a, figure 1) and a second memory controller (24b, figure 1), the memory request arbiter including a first arbiter (59A, figure 2) coupled to the first memory controller and a second arbiter (59B, figure 2) coupled to the second memory controller, wherein the first arbiter and the second arbiter perform real time scheduling of memory requests (column 18, lines 34 – 38).

It would have been obvious to one of ordinary skill in the art at the time of the Applicant's invention to utilize the dual memory controller/interface of Ottinger in the above mentioned teachings of Hook. One of ordinary skill would be motivated to make such modification in order to increase the performance of the system by reducing the average latency of memory requests (column 2, lines 10 – 25).

Response to Arguments

16. Applicant's arguments with respect to claim 4 - 11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on (571)272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

HENRY TSAI
SUPERVISORY PATENT EXAMINER

1/5/08